REMARKS

Claims 1-4, 6-10, 12-24, 26 and 27 are currently pending in the subject application and are presently under consideration. Applicants' representative thanks the Examiner for the teleconference of August 14, 2007. The rejections under 35 U.S.C. §103(a) were discussed.

Favorable reconsideration of the subject patent application is respectfully requested in view of the comments herein.

I. Rejection of Claims 1-4, 6-10, 12-14, 17-24, & 26 Under 35 U.S.C. §102(e)

Claims 1-4, 6-10, 12-14, 17-24, & 26 stand rejected under 35 U.S.C. §102(e) as being anticipated by VanBuskirk, *et al.* US 2003/0208663A1.

> A single prior art reference anticipates a patent claim only if it ***expressly or inherently describes each and every limitation set forth in the patent claim***. *Trintec Industries, Inc. v. Top-U.S.A. Corp.,* 295 F.3d 1292, 63 USPQ2d 1597 (Fed. Cir. 2002); *See Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The ***identical invention must be shown in as complete detail as is contained in the ... claim***. *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) (emphasis added).

The claimed invention relates to on-chip placement of referencing circuitry in a multi-bit memory device. In particular, independent claim 1 recites an architecture that facilitates a reference voltage in a multi-bit memory, comprising a multi-bit memory core including a plurality of data cells for storing data; *first and second reference arrays fabricated adjacent to each other and associated with one of a plurality of sectors comprising multi-bit data cells,* ***the first and second reference arrays each comprised of a plurality of multi-bit reference cells fabricated on the memory core,*** *wherein reference cells within the first reference array have a first voltage level and reference cells within the second reference array have a second voltage level,* ***the second voltage level different than the first voltage level***; and a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage employed during a data cell read operation. Independent claims 13, 17 and 24 recite similar aspects. Van Buskirk *et al.* does not disclose such aspects of the subject claims.

Van Buskirk *et al.* relates to reading multi-bit flash memory devices. At Page 3 of the Final Office Action, the Examiner incorrectly asserts that the cited reference fabricates reference arrays ***on the memory core***, as afforded by independent claim 1. To the contrary, the reference disposes reference arrays external to the memory core.

Moreover, Van Buskirk *et al.* fails to disclose that reference cells within the first reference array have a first voltage level and reference cells within the second reference array have a second voltage level, ***the second voltage level different than the first voltage level***. At Page 3 of the Final Office Action, the Examiner incorrectly asserts that it must be used two different voltages to form an average as disclosed in Figure 5 of Van Buskirk *et al.* Van Buskirk *et al.* discloses determining the reference voltage by averaging the first voltage level of the first reference array and the second voltage level of the second reference array. However, Van Buskirk *et al.* is completely silent regarding ***the second voltage level different than the first voltage level*** as recited in the subject claim. Even if two voltage levels of the first reference array and the second reference array are the same, the system disclosed in Van Buskirk *et al.* can do the average of the reference voltage by adding the same voltages and divide them by two. Thus, the same voltage levels of the first reference array and the second reference array disclosed in Van Buskirk *et al.* can be used to form an average. Van Buskirk *et al.* can determine the reference voltage by averaging the first voltage level of the first reference array and the second voltage level of the second reference array even if ***the second voltage level is the same as the first voltage level***. On the contrary, the subject claim determines the reference voltage by averaging the first voltage level of the first reference array and the second voltage level of the second reference array, ***the second voltage level different than the first voltage level***. Thus, when determining dynamically the reference voltage by averaging select ones of the respective first and second reference cells, the derived reference voltage is more accurate with respect to the data bit values of the data sectors.

The Examiner seems to reply on the theory of inherency to assert that the second voltage level is different than first second voltage level. However, " to establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " *In re Robertson*,

169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). The voltage level difference of the first reference array and the second reference array disclosed in the subject claim is not necessarily present in the thing described in Van Buskirk *et al.*

In view of at least the foregoing, it is readily apparent that Van Buskirk *et al.* does not teach the identical invention in as complete detail as is contained in the subject claims. Accordingly, this rejection with respect to independent claims 1, 13, 17 and 24 (and the claims that depend from) should be withdrawn.

II. Rejection of Claim 15 Under 35 U.S.C. §103(a)

Claim 15 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Van Buskirk, *et al.* US 2003/0208663A1 in view of Ferrant US 6,538,942. This rejection should be withdrawn for at least the following reasons.

Patent No. US 2003/0208663A1 is not citable prior art with respect to the present application. The following is a quotation of 35 U.S.C. §103(c), which forms at least one basis for withdrawal of this rejection:

> (c) Subject matter developed by another person, which qualifies as prior art only under subsection (e), (f), and or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

The subject matter of Patent No. US 2003/0208663A1 and the claimed invention were, at the time the invention was made, subject to an obligation of assignment to Advanced Micro Devices, Inc. Therefore, the subject matter of Patent No. US 2003/0208663A1 is not a citable reference with respect to the subject application, and withdrawal of this rejection is respectfully requested.

III. Rejection of Claims 16 & 27 Under 35 U.S.C. §103(a)

Claims 16 & 27 stand rejected under 35 U.S.C. §103(a) as being unpatentable as being unpatentable over Van Buskirk, *et al.* US 2003/0208663A1 in view of Kurihara *et al.* US 6,791,880. Applicants' representative respectfully requests withdrawal of this rejection for at

least the following reasons.

As described above, the subject matter of Patent No. US 2003/0208663A1 and the claimed invention were, at the time the invention was made, subject to an obligation of assignment to Advanced Micro Devices, Inc. Therefore, the subject matter of Patent No. US 2003/0208663A1 is not a citable reference with respect to the subject application, and withdrawal of this rejection is respectfully requested.

CONCLUSION

The present application is believed to be in condition for allowance in view of the above comments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [AMDP975US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

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